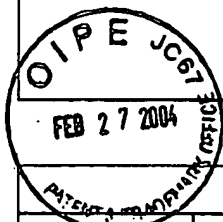


<b>FORM 1449*</b> <b>INFORMATION DISCLOSURE STATEMENT</b>  <b>IN AN APPLICATION</b> (Use several sheets if necessary)	Docket Number: 10873.1358US01	Application Number: 10/730,839
	Applicant: OZASA, et al.	
	Filing Date: December 8, 2003	Group Art Unit: <del>Unknown</del> 2816



U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
BT	2-124609	May, 1990	Japan	—	—	abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
BT		"Semiconductor Circuit Design Technology", Nikkei Business Publishers Inc., edited by T. Tamai, 1st edition, p. 302
BT		"CMOS Analog Circuit Design Second Edition", p. 196, published by OXFORD, Phillip E. Allen and Douglas R. Holberg

23552 PATENT TRADEMARK OFFICE		DATE CONSIDERED	3/3/05
EXAMINER		EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form for next communication to the Applicant.	